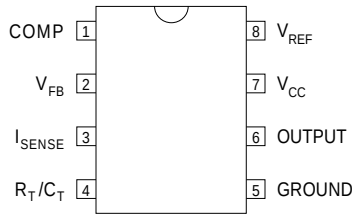
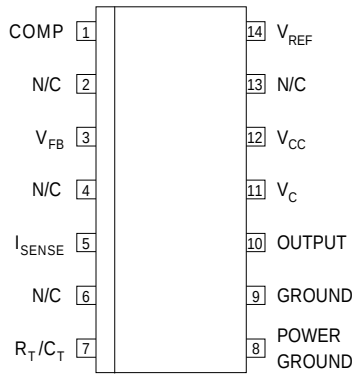
IP1842 SERIES
IP1843 SERIES

TOP VIEW



J Package – 8 Pin Ceramic DIP
N Package – 8 Pin Plastic DIP
D-8 Package – 8 Pin Plastic (150) SOIC

TOP VIEW



D-14 Package – 14 Pin Plastic (150) SOIC

CURRENT MODE REGULATING PULSE WIDTH MODULATORS

FEATURES

- **Guaranteed ±1% reference voltage tolerance**
- **Guaranteed ±10% frequency tolerance**
- **Low start–up current (<500 µA)**
- **Under voltage lockout with hysteresis**
- **Output state completely defined for all supply and input conditions**
- **Interchangeable with UC1842 and UC1843 series for improved operation**
- **500kHz operation**

Order Information

Part Number	J–Pack 8 Pin	N–Pack 8 Pin	D–8 8 Pin	D–14 14 Pin	Temp. Range
IP1842	✔				-55 to +125°C
IP2842	✔	✔	✔	✔	-25 to +85°C
IP3842	✔	✔	✔	✔	0 to +70°C
IP1843	✔				-55 to +125°C
IP2843	✔	✔	✔	✔	-25 to +85°C
IP3843	✔	✔	✔	✔	0 to +70°C

Note:

To order, add the package identifier to the part number.

eg. IP1842J
IP3843D-14

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

V_{CC}	Supply Voltage	(low impedance source) (I_{CC} < 30mA)	+30V Self limiting
I_O	Output Current		±1A
	Output Energy	(capacitive load)	5µJ
	Analog Inputs	(pins 2 and 3)	–0.3V to +V_{CC}
	Error Amp Output Sink Current		10mA
P_D	Power Dissipation Derate @ T_{amb} > 50°C	T_{amb} = 25°C	1W 10mW/°C
P_D	Power Dissipation Derate @ T_{case} > 25°C	T_{case} = 25°C	2W 24mW/°C
T_{STG}	Storage Temperature Range		–65 to 150°C
T_L	Lead Temperature	(soldering, 10 seconds)	+300°C

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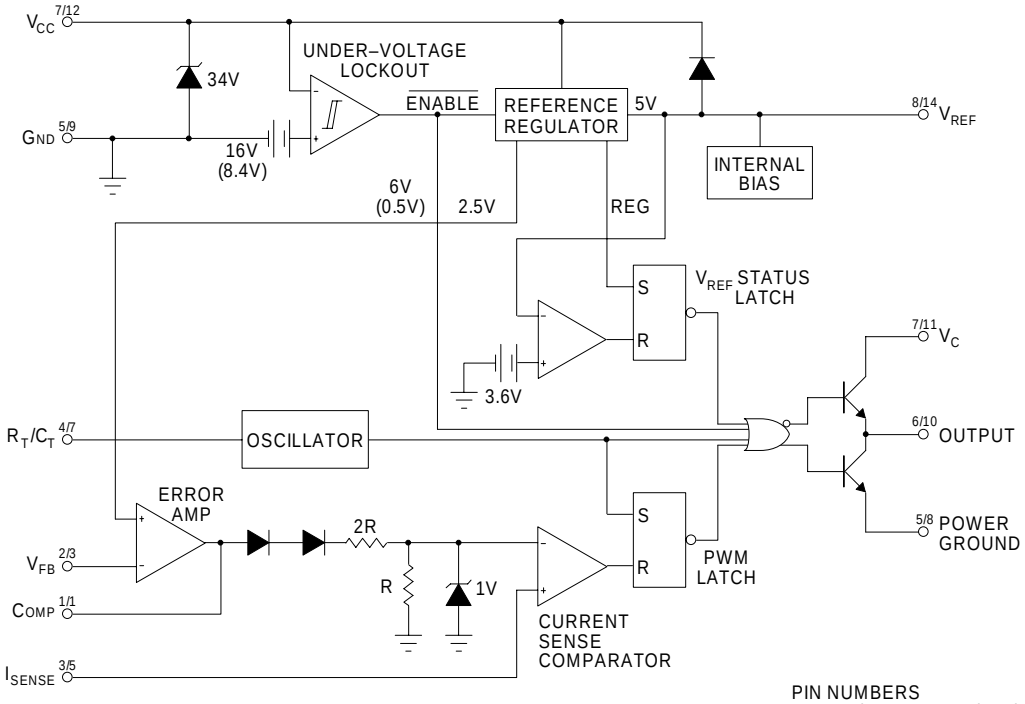
IP1842 SERIES
IP1843 SERIES

DESCRIPTION

The IP1842 and IP1843 series of switching regulator control circuits contain all the functions necessary to implement off–line, current mode switching regulators, using a minimum number of external parts. Functions included are voltage reference, error amplifier, current sense comparator, oscillator, totem pole output driver and under-voltage lockout circuitry.

Although pin compatible with the UC1842 and 1843 series, SEMELAB has incorporated several improvements in the IP1842 and IP1843 series allowing tighter and more complete specification of electrical performance.

BLOCK DIAGRAM



Values in brackets are for IP1843 series.

PIN NUMBERS
1st Number – N, J and 8 Pin D Packages
2nd Number – 14 Pin D Package.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply Voltage [1]		≤ 30V
I_O	Output Current		0 to ±200mA
	Analog Inputs (pins 2 and 3)		–0.3V to 3V
	Error Amp Output Sink Current		0 to 2mA
	Operating Ambient Temperature Range	IP1842 , IP1843	–55 to 125°C
		IP2842 , IP2843	–25 to 85°C
		IP3842 , IP3843	0 to 70°C

Notes:

1. Lower limit set by under voltage lockout specification.

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ELECTRICAL CHARACTERISTICS (Over Full Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions	IP1842/IP1843 IP2842/IP2843 Min.	Typ.	Max.	IP3842 IP3843 Min.	Typ.	Max.	Units
	REFERENCE SECTION							
Output Voltage	I_O = 1mA T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Input Regulation	V_{CC} = 12V to 25V		6	20		6	20	mV
Output Regulation	I_O = 1mA to 20mA		6	25		6	25	
Temperature Stability			0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp	4.90		5.10	4.82		5.18	V
Output Noise Voltage	f = 10Hz to 10kHz T_J = 25°C		50			50		µV
Long Term Stability	T_J = 125°C @ 1000Hrs		5	25		5	25	mV
Output Short Circuit Current	V_{REF} = 0	30	80	160	30	80	160	mA
	OSCILLATOR SECTION							
Frequency	T_J = 25°C	47	52	57	47	52	57	kHz
Voltage stability	V_{CC} = 12V to 25V		0.2	1		0.2	1	%
Temperature Stability	ΔT_A = Min to Max		5			5		%
Amplitude	V_{PIN4} Peak to Peak		1.7			1.7		V
Discharge Current	T_J = 25°C		8.3			8.3		mA
	ΔT_A = Min to Max		8			8		%
	ERROR AMP SECTION							
Input Voltage	V_{PIN1} = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			–0.3	–1		–0.3	–2	µA
Open Loop Voltage Gain	V_O = 2V to 4V	65	90		65	90		dB
Unity Gain Bandwidth		0.7	1		0.7	1		MHz
Supply Voltage Rejection	V_{CC} = 12V to 25V	60	70		60	70		dB
Output Sink Current	V_{PIN2} = 2.7V V_{PIN1} = 1.1V	2	6		2	6		mA
Output Source Current	V_{PIN2} = 2.3V V_{PIN1} = 4.6V	–0.5	–0.8		–0.5	–0.8		
V_{OUT} High	V_{PIN2} = 2.3V R_L = 15kΩ	4.6	4.8		4.6	4.8		V
V_{OUT} Low	V_{PIN2} = 2.7V R_L = 15kΩ		0.7	1.1		0.7	1.1	

NOTES

1. Test Conditions unless otherwise stated:
   V_{CC} = 15V* , R_T = 10kΩ , C_T = 3.3nF , f = 52kHz.
   *Adjust V_{CC} above start threshold before setting at required level.

   All specifications apply over the full operating temperature range unless otherwise stated. (See Ordering Information for further details).

ELECTRICAL CHARACTERISTICS (Over Full Operating Temperature Range unless otherwise stated)

Parameter	Test Conditions		IP1842/IP1843 IP2842/IP2843 Min.	Typ.	Max.	IP3842 IP3843 Min.	Typ.	Max.	Units
	CURRENT SENSE SECTION								
Gain	See Notes 2,3		2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	V_{PIN1} = 4.6V	(Note 2)	0.9	1	1.1	0.9	1	1.1	V
Supply Voltage Rejection	V_C = 12V to 25V		60	70		60	70		dB
Input Bias Current				–2	–10		–2	–10	µA
Delay to Output				200	400		200	400	ns
	OUTPUT SECTION								
Output Low Level	I_{SINK} = 20mA			0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA			1.5	2.2		1.5	2.2	
Output High Level	I_{SOURCE} = 20mA		13	13.5		13	13.5		V
	I_{SOURCE} = 200mA		12	13.5		12	13.5		
Rise Time	C_L = 1nF	T_J = 25°C		50	150		50	150	ns
Fall Time	C_L = 1nF	T_J = 25°C		50	150		50	150	
UVLO Saturation	V_{CC} = 6V	I_L = 1mA		0.7	1.1		0.7	1.1	V
	UNDER–VOLTAGE LOCKOUT SECTION								
Upper Threshold (V_{CC})	1842 Series		15	16	17	14.5	16	17.5	V
	1843 Series		7.8	8.4	9	7.8	8.4	9	
Lower Threshold (V_{CC})	1842 Series		9	10	11	8.5	10	11.5	V
	1843 Series		7	7.6	8.2	7	7.6	8.2	
	TOTAL STANDBY CURRENT								
Start–up Current				0.3	0.5		0.3	0.5	mA
Operating Supply Current	V_{PIN2} = 0V	1842 Series		11	15		11	15	mA
	V_{PIN3} = 0V	1843 Series		14	17		14	17	
V_{CC} Zener Voltage	I_{CC} = 25mA		30	34	40	30	34	40	V

NOTES

1. Test Conditions unless otherwise stated:
   V_{CC} = 15V* , R_T = 10kΩ , C_T = 3.3nF , f = 52kHz.
   *Adjust V_{CC} above start threshold before setting at required level.

   All specifications apply over the full operating temperature range unless otherwise stated.
   (See Ordering Information for further details).

2. Parameter measured at trip point of latch with V_{PIN2} = 0V

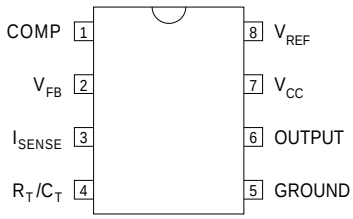
3. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}}$$

$$0 \le V_{PIN3} \le 0.8$$

APPLICATIONS INFORMATION

Oscillator Waveforms and Maximum Duty Cycle



Oscillator timing capacitor C_T is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of R_T and C_T therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulae:

$t_c \approx 0.55\ R_T C_T$

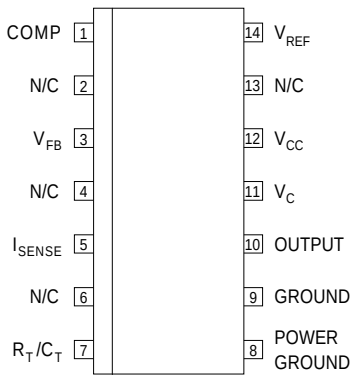
$t_d \approx R_T C_T\ \ell n \left(\frac{.0063\ R_T - 2.3}{.0063\ - 4}\right)$

Resultant frequency $f = \frac{1}{(t_c + t_d)}$

For $R_T > 5k\Omega$,

Resultant frequency $f \approx \frac{1.8}{(R_T C_T)}$

Open–Loop Laboratory Test Fixture



High peak current associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5K potentiometer are used to sample the oscillator wave form and apply an adjustable ramp to pin 3.

TYPICAL PERFORMANCE CHARACTERISTICS